



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/294,617	04/19/1999	ANDREW T. JENNINGS	TN137	6329

7590

08/25/2005

STEVEN B SAMUELS ESQ  
UNISYS CORPORATION  
TOWNSHIP LINE & UNION MEETING ROADS  
BLUE BELL, PA 19424

EXAMINER

KENDALL, CHUCK O

ART UNIT

PAPER NUMBER

2192

DATE MAILED: 08/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/294,617

Applicant(s)

JENNINGS ET AL.

Examiner

Chuck O. Kendall

Art Unit

2192

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 27 May 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 32 and 33 is/are allowed.
- 6) ☐ Claim(s) \_\_\_\_\_ is/are rejected.
- 7) ☒ Claim(s) 16,17 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

***Detailed Action***

1. This action is in response to the application filed 05/27/05.
2. Claims 1 – 33 are pending.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1, 2, 4, 5, 9, 10,12,13,19,20, 22,23,29 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Lethin et al. USPN 6,463,582 B1.

With regards to claim 1, Lethin anticipates a system (FIG.23), method (Col.2: 17-30), product (Col.2: 17 – 30) (for emulating (2:17) the execution of a target program comprising instructions of an instruction set of a target computer on a host computer having a different instruction set, said method comprising; performing a static translation (50:12 – 17) of the instructions of the target program into a series of instructions of an intermediated instruction set, the intermediate instruction set being optimized for interpretation on the host computer (50:12 – 17); executing the series of instructions of the intermediate instruction set by interpretation directly by the host computer (2:45 – 57).

Regarding claim 2, wherein the intermediate instruction set comprises a plurality of control words that are derived, at least in part, by mapping control words of the instruction set of the target machine into the fundamental word size of the host machine (25:40 – 55).

Regarding claim 4, as recited in claim 1, wherein the intermediate instruction set comprises a plurality of different types of control words having formats defined to minimize the time needed to determine the type of a control word (25:40 – 55, for different control words see types supported 8, 16 and 32 bits).

With regards to claim 5, as recited in claim 1 wherein the intermediate instruction set comprises a plurality of control words derived from control words of the instruction set of the target machine in a manner that reduces the number of different forms of control words in the intermediate instruction set (25:55 – 57, see eliminating redundant loads and stores).

Regarding claim 9, which is the system version of the method in claim 1, see rationale as discussed above.

Regarding claim 10, which is the system version of the method in claim 2, see rationale as discussed above.

Regarding claim 12, which is the system version of the method in claim 4, see rationale as discussed above.

Regarding claim 13, which is the system version of the method in claim 5, see rationale as discussed above.

Regarding claim 19, which is the computer readable version of the method in claim 1, see rationale as discussed above.

Regarding claim 20, recites similarly as claim 1, see rationale as discussed above.

Regarding claim 22, which is the computer readable version of the method in claim 4, see rationale as discussed above.

Regarding claim 23, which is the computer readable version of the method in claim 5, see rationale as discussed above.

Regards, to claim 29 see reasoning in claim 4.

Regarding claim 32, recites similarly as claim 1, see rationale as discussed above.

6. Claims 3, 21 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lethin et al. USPN 6,463,582 B1 as applied in claims 1, in view of Chin et al. USPN 5,581,778.

With regards to claim 3, Lethin discloses all the claimed limitations as applied in claim 1. Lethin doesn't explicitly disclose redefining control words of the target computer to minimize the number of masking and shifting operations. However Chin does disclose this in an analogous art and similar configuration performing mask and shifting operations (30:28 - 45). Therefore it would have been obvious to one of ordinary skill art at the time the invention was made to combine Lethin with Chin because,

Art Unit: 2192

enabling a reduction in the shifts and masks prevents interference between several independent IPC operations (30:25 – 30).

Regarding claim 21, which is the computer readable version of the method in claim 3, see rationale as discussed above.

Regards, to claim 28 see reasoning in claim 3.

7. Claims 6 – 8, 14, 15 and 18,24 – 26, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lethin et al. USPN 6,463,582 B1 as applied in claims 1, in view of Yates, Jr et al. USPN 6,397,379 B1.

With regards to claim 6, Lethin discloses all the claimed limitations as applied in claim 1. Lethin doesn't explicitly disclose wherein the instructions of the intermediate instruction set have a fixed length and do not cross code word boundaries. However Yates discloses fixed mappings between instructions sets (24:35 – 40). Therefore it would have been obvious to one of ordinary skill art at the time the invention was made to combine Lethin and Yates because, using fixed length during instruction mapping would enable the instructions from the host to the target architecture to be constant and hence mapped more efficiently.

8. Claims 6 – 8, 14, 15 and 18,24 – 26, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lethin et al. USPN 6,463,582 B1 as applied in claims 1, in view of Gee et al. USPN 6,317,872 B1.

With regards to claim 7, Lethin discloses all the claimed limitations as applied in claim 1. Although, Lethin doesn't explicitly disclose wherein zero-address instructions of the instruction set of the target machine for pushing data onto a stack for use in a subsequent zero-address instruction operation, Lethin does use a stack-oriented structure to (43:63 – 67). However, Gee does disclose a stack-oriented architecture, which uses Last-in First-out storage, which is often referred to as “zero address”. Therefore it would have been obvious to one of ordinary skill art at the time the invention was made to combine Lethin with Gee because, using zero instructions for subsequent, zero address instructions would enable allocation in a stack oriented architecture.

Regarding claim 14, which is the system version of the method in claim 6, see rationale as discussed above.

Regarding claim 15, which is the system version of the method in claim 7, see rationale as discussed above.

Regarding claim 18, which is the system version of the method in claim 8, see rationale as discussed above.

Regarding claim 24, which is the computer readable version of the method in claim 6, see rationale as discussed above.

Regarding claim 25, which is the computer readable version of the method in claim 7, see rationale as discussed above.

Regarding claim 26, which is the computer readable version of the method in claim 8, see rationale as discussed above.

Regards, to claim 30 see reasoning in claim 6.

Regards, to claim 31 see reasoning in claim 8.

***Allowable subject matter***

9. Claims 16, 17, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims..

“...wherein the code translator runs as a user mode process under control of a host operating system on the host computer, and wherein the interpreter runs as a kernel mode driver thread under the host operating system”.

“...wherein the emulation system may comprise multiple instances of the interpreter each running as a different thread in the kernel space of the host operating system”.

10. Regarding Claims 32 and 33, the prior art of record does not teach or fairly suggest at least:

“...wherein the emulation system may comprise multiple instances of the interpreter each running as a different thread in the kernel space of the host operating system”.



Therefore, claims 32 and 33 is in condition for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

### ***Response to Arguments***

11. Applicant's arguments with respect to claims 1 - 31 have been considered but are moot in view of the new ground(s) of rejection.


### **Correspondence information**

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuck Kendall whose telephone number is 571-272-3698. The examiner can normally be reached on 10:00 am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ck.



**TUAN DAM**  
**SUPERVISORY PATENT EXAMINER**